REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-30 are presently active in this case. The present Amendment amends Claims 1-6, 16-22, 26 and 30 without introducing any new matter and cancels Claims 31-46.

The outstanding Office Action rejected Claims 1-2 and 6 under 35 U.S.C. §102(b) as anticipated by Applicants' Figures 6-8. Claims 3-5 were rejected under 35 U.S.C. §103(a) as unpatentable over Figures 6-8 as applied to Claim 1 above and further in view of Harada et al. (U.S. Patent Publication No. 2001/0008311, herein "Harada"). Claims 7-15 were rejected under 35 U.S.C. §103(a) as unpatentable over Figures 6-8 as applied to Claim 1 above, and further in view of Noda et al. (U.S. Patent No. 6,731,538, herein "Noda").

Claims 16-30 were allowed. Applicants acknowledge with appreciation the indication of allowable subject matter.

In response to the rejection of Claims 1-2 and 6 under 35 U.S.C. §102(b), independent Claim 1 is amended to recite a first memory cell including a first gate electrode and first and second diffusion layers, a second memory cell including a second gate electrode and third and fourth diffusion layers, and a second bit line. Claim 1 is further amended to recite "the first and second memory cells arranged in a direction perpendicular to the first bit line." The amendments to Claim 1 find support in Applicants' original specification from page 3, line 21 to page 4, line 36 and in corresponding Figures 1-3. Figures 1-2 are cross-sectional views of the semiconductor memory device represented in Figure 3.[1]

Figure 1 shows a cross section through a memory element region ER, Figure 2 shows a cross-section through a word line WL2 and Figure 3 shows a top view of the semiconductor

[1] See Applicants' specification at page 6, lines 6-12.

memory device. Figure 3 shows first and second memory cells (element regions ER) and Figure 1 shows first and second gate electrodes (204-209) as well as the first, second, third and fourth diffusion layers (301). The first and second bit lines are shown in Figure 1 (215). Further, from Figure 1-3 it can be seen that the second gate electrode of the second memory cell is electrically connected to the first gate electrode of the first memory cell and also that the first and second memory cells are arranged in a direction *perpendicular* to the first bit line (Figure 3). Additionally, Figure 2 and Figure 3 show that the second gate electrode and the second memory cell are electrically connected to the first gate electrode of the first memory cell. Since the amendments to Claim 1 find support in the Specification and in the Figures as originally filed, these changes are not believed to raise any question on new matter.[2] Additionally, dependent Claims 2-6 are amended to cancel "having a gate electrode and a diffusion layer" from the preamble, in accordance with the amendments to independent Claim 1.

Independent Claim 16 has also been amended to change "the semiconductor memory device" to "the plurality of memory cells." Dependent Claims 17-22, 26 and 30 are amended to delete "having a gate electrode and a diffusion layer" from the preamble and/or to replace "the semiconductor memory device" with "the plurality of memory cells" for consistency. In light of their formal nature, the changes to the Specification and Abstract do not raise a question of new matter.

The Specification and the Abstract of the disclosure are amended in accordance with the changes to independent Claim 1. These amendments are supported in the Specification and in the Figures as originally filed as discussed above and therefore do not raise a question of new matter.

[2] See MPEP 2163.06 stating that "information contained in any one of the specification, claims or drawings of the application as filed may be added to any other part of the application without introducing new matter."

Briefly recapitulating, Applicants' invention, as recited in amended Claim 1, relates to a semiconductor memory device, including a first contact layer connected to the first diffusion layer of the first memory cell, a second contact layer connected to the first contact layer, and a first bit line connected to the second contact layer and arranged above the first gate electrode of the first memory cell. The second contact layer is electrically connected to the bit line. Further, first and second memory cells are arranged in a direction perpendicular to the first bit line.

The outstanding Office Action states that the claimed first and second contact layers correspond to the metal "layer" 116 and the source contact 102b and metal "layer" 114b and source line 103, respectively, with respect to Applicants' Figures 6-8.[3] Applicants respectfully disagree. As recited in amended Claim 1, the first and second contact layers are distinct layers. The first contact layer is connected to the first diffusion layer, and the second contact layer is electrically connected to the bit line.

By contrast, as shown in Figure 6, first, the segment 103/114b/102b/116 is not connected to the bit line, so it cannot correspond to the second contact layer. Second, Figure 6 shows a single layer (103/114b/102b/116), so even if it were connected between a drain region of the upper semiconductor surface 100 and a bit line 115,[4] the claimed "first" and "second" contact layers would not be present. Third, the feature "a height of the conductive layer substantially being coplanar with a height of the first contact layer," as recited in Applicants' original Claim 1, is also ***neither taught nor suggested*** by Applicants' Figures 6-8. Since 114a is the first contact layer in Figure 6, its height is not substantially coplanar with the height of a conductive layer since the corresponding conductive layer in Figure 6 is 103.

[3] See outstanding Office Action at page 2, lines 14-16.
[4] See Applicants' specification at page 1, lines 21-24 and in Figure 6.

Thus, as taught by Applicants, when creating the structure of Figure 6, a contact hole is formed with a depth of the total thickness of the source line 103 and the silicon oxide layer 113, in order to fill the metal in the contact hole, and that such an effect leads to a poor conduction between the metal and the contact hole.[5]

In response to the rejections of Claims 3-5 and 7-15 under 35 U.S.C. §103(a), Applicants traverse these rejections and request reconsideration of these rejections, as next discussed.

As stated above in the arguments towards the 35 U.S.C. §102(b) rejection, the applied references (Harada as well as Noda) ***do not teach or suggest*** all the features recited in amended Claim 1. In addition to the features not taught or suggested by Applicants' Figures 6-8, Harada ***neither teaches nor suggests*** Applicants' claimed "bit line," "a first memory cell," and "a second memory cell," as would be required to meet the features recited in amended Claim 1. Harada merely teaches that a gold or aluminum wire 30 is bonded to the pad electrode 26.[6] Again, Applicants' Figures 6-8 do not teach or suggest the features of amended Claim 1 and the Noda reference ***does not*** teach (or suggest) an arrangement of memory cells, such as the claimed arrangement of a "first memory cell" and a "second memory cell."

Therefore, even if the combination of the teachings of Applicants' Figures 6-8 with the Harada or Noda reference is assumed to be proper, the combination fails to teach every element of the claimed invention. Specifically, the combination fails to teach the claimed first and second memory cells. Accordingly, Applicants respectfully traverse, and request reconsideration of, these rejections based on these patents.[7]

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[5] See Applicants' specification at page 3, lines 8-14.
[6] See Harada at page 6, paragraph 107, lines 4-8 and in Figure 2K.
[7] See MPEP 2142 stating, as one of the three "basic criteria [that] must be met" in order to establish a *prima facie* case of obviousness, that "the prior art reference (or references when combined) must teach or suggest all

The present amendment is submitted in accordance with the provisions of 37 C.F.R. §1.116, which after Final Rejection permits entry of amendments placing the claims in better form for consideration on appeal. As the present amendment is believed to overcome outstanding rejections under 35 U.S.C. §102(b) and 35 U.S.C. §103(a), the present amendment places the application in better form for consideration on appeal. In addition, the present amendment is not believed to raise new issues because the changes to independent Claim 1 are for clarification purposes and replaces the expression "vertical" with "perpendicular." Further, the changes to independent Claim 16 are of a minor nature. It is therefore respectfully requested that 37 C.F.R. §1.116 be liberally construed, and that the present amendment be entered.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal Allowance. A Notice of Allowance for Claims 1-30 is earnestly solicited.

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the claim limitations," (emphasis added). See also MPEP 2143.03: "All words in a claim must be considered in judging the patentability of that claim against the prior art."

Should the Examiner deem that any further action is necessary to place this application in even better form for allowance, the Examiner is encouraged to contact Applicants' undersigned representative at the below listed telephone number.

Respectfully submitted,

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